UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,288	10/24/2003	Heon Lee	200209574-1	2350

22879 7590 06/10/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,288	LEE, HEON	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *13-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-19* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12, drawn to a method, classified in class 438, subclass 720.

II. Claims 13-19, drawn to a device, classified in class 257, subclass 295.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, a magnetic tunnel junction device can be manufactured without using the damascene process and or reactive ion etching. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper. Furthermore, because the search required for Invention I is not required for Invention II, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Brian Short on June 2, 2005, a provisional election was made without traverse to prosecute Invention I claims 1-12. Affirmation of this election must be made by applicant in replying to this Office action. Claims 13-19 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Priority

4. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. *See In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

6. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

7. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-12 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 5, 7-11, 15, and 17-20 of copending Application No. 10/692,773, filed Oct. 24, 2003, Lee ("Lee I") (U.S. Patent Appl. Pub. No. 2005/0090111). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

9. As to claim 1, Lee I claims a method of making a magnetic tunnel junction device (Application No. 10/692,773, filed Oct. 24, 2003, claim 1, page 21, line 3), comprising: forming a magnetic tunnel junction stack (claim 1, page 21, line 5); forming a first mask layer on the magnetic tunnel junction stack (claim 1, page 21, line 10); patterning the first mask layer (claim 1, page 21, line 12); forming a discrete magnetic tunnel junction stack by etching the first mask layer (claim 1, page 21, line 14-15); forming an electrically non-conductive spacer layer on the discrete magnetic tunnel junction stack (claim 1, page 21, lines 17-18); forming a spacer by anisotropically etching the spacer layer (claim 1, page 21, line 20); forming a dielectric layer over the discrete magnetic tunnel junction stack and the spacer (claim 1, page 21, line 22-23); planarizing the dielectric layer to form a substantially planar surface (claim 1, page 21, lines 25-26); forming a self-aligned via by etching away the first mask layer (claim 1, page 21, line 28); depositing a first electrically conductive material on the dielectric layer and in the self-aligned via (claim 1, page 21, lines 30-31); patterning the first electrically conductive material (claim 1, page 22, line 1); and forming a dual-damascene conductor by etching the first electrically conductive material (claim 1, page 22, lines 3-4).

10. Although the conflicting claims are not identical, they are not patentably distinct from each other because Applicant's claim 1 is generic to all that is recited in claim 1 of Lee I in Application No. 10/692,773. That is, claim 1 of Lee I falls entirely within the scope of Applicants' claim 1 or, in other words, Applicants' claim 1 is anticipated by claim 1 of Lee I. Specifically, Lee I's claim 1 contains additional limitations, such as forming an etch stop layer on the magnetic tunnel junction stack, the etch stop layer comprising a first electrically conductive material (claim 1, page 21, lines 7-8), which are not claimed by the Applicant.

11. As to claim 2, Lee I claims that the depositing of the first electrically conductive material is continued until the first electrically conductive material completely fills the self-aligned via and the first electrically conductive material extends outward of the substantially planar surface by a predetermined distance (claim 5, page 22, lines 16-19).

12. As to claim 3, Lee I claims that the spacer layer is conformally deposited on the discrete magnetic tunnel junction stack (claim 7, page 22, lines 25-26).

13. As to claim 4, Lee I claims that the spacer layer comprises a material selected from the group consisting of silicon oxide and silicon nitride (claim 8, page 22, lines 28-29).

14. As to claim 5, Lee I claims that the anisotropically etching the spacer layer comprises a reactive ion etch (claim 9, page 22, lines 31-32).

15. As to claim 6, Lee I claims that after the forming of the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other (claim 10, page 23, lines 1-3).

16. As to claim 7, Lee I claims a method of making a magnetic tunnel junction device from a previously fabricated discrete magnetic tunnel junction stack (claim 11, page 23, lines 5-6), comprising: forming an electrically non-conductive spacer layer on the previously fabricated discrete magnetic tunnel junction stack (claim 11, page 23, lines 18-19); forming a spacer by anisotropically etching the spacer layer (claim 11, page 23, lines 21); forming a dielectric layer over the previously fabricated discrete magnetic tunnel junction stack and the spacer (claim 11, page 23, lines 23-24); planarizing the dielectric layer to form a substantially planar surface (claim 11, page 23, lines 26-27); forming a self-aligned via by etching away a first mask layer of the previously fabricated discrete magnetic tunnel junction stack (claim 11, page 23, line 29); depositing a first electrically conductive material on the dielectric layer and in the self-aligned via (claim 11, page 23, line 31); patterning the first electrically conductive material (claim 11, page 24, line 3); and forming a dual-damascene conductor by etching the first electrically conductive material (claim 11, page 24, lines 5-6).

17. Although the conflicting claims are not identical, they are not patentably distinct from each other because Applicant's claim 7 is generic to all that is recited in claim 11 of Lee I in Application No. 10/692,773. That is, claim 11 of Lee I falls entirely within the scope of Applicants' claim 7 or, in other words, Applicants' claim 7 is anticipated by claim 11 of Lee I. Specifically, Lee I's claim 11 contains additional limitations, such as

forming an etch stop layer (claim 11, page 23, lines 8-9) and forming and patterning a first mask layer (claim 11, page 21, lines 11 and 13), which are not claimed by the Applicant.

18. As to claim 8, Lee I claims that the depositing of the first electrically conductive material is continued until the first electrically conductive material completely fills the self-aligned via and the first electrically conductive material extends outward of the substantially planar surface by a predetermined distance (claim 15, page 24, lines 19-22).

19. As to claim 9, Lee I claims that the spacer layer is conformally deposited on the previously fabricated discrete magnetic tunnel junction stack (claim 17, page 24, lines 28-29).

20. As to claim 10, Lee I claims that the spacer layer comprises a material selected from the group consisting of silicon oxide and silicon nitride (claim 18, page 24, lines 31-32).

21. As to claim 11, Lee I claims that the anisotropically etching the spacer layer comprises a reactive ion etch (claim 19, page 25, lines 1-2).

22. As to claim 12, Lee I claims that after the forming of the self-aligned via, the previously fabricated discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other (claim 20, page 25, lines 4-6).

23. Claims 1-12 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-12 of copending Application No. 10/692,612, filed Oct. 24, 2003, Lee ("Lee II") (U.S. Patent

Appl. Pub. No. 2005/0090056), in view of Costrini et al. (U.S. Patent Appl. Pub. No. 2004/0063223). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

24. As to claim 1, Lee II claims a method of making a magnetic tunnel junction device (Applicant's Amendments to the Claims, filed Jan. 31, 2005, claim 1, page 3, lines 6-7), comprising: forming a magnetic tunnel junction stack (page 3, line 9); forming a discrete magnetic tunnel junction stack (claim 1, page 3, line 13-14); forming an electrically non-conductive spacer layer on the discrete magnetic tunnel junction stack (claim 1, page 3, line 16-17); forming a spacer by anisotropically etching the spacer layer (claim 1, page 3, line 19); forming a dielectric layer over the discrete magnetic tunnel junction stack and the spacer (claim 1, page 3, line 21-22); planarizing the dielectric layer to form a substantially planar surface (claim 1, page 3, line 24); forming a self-aligned via by etching (claim 1, page 3, line 28); depositing a first electrically conductive material on the dielectric layer and in the self-aligned via (claim 1, page 3, line 30-31); patterning the first electrically conductive material (claim 1, page 4, line 7); and forming a dual-damascene conductor by etching the first electrically conductive material (claim 1, page 4, line 9).

25. Lee II does not expressly claim forming a first mask layer on the magnetic tunnel junction stack; patterning the first mask layer; forming a discrete magnetic tunnel junction stack by etching the first mask layer; and forming a self-aligned via by etching away the first mask layer. However, Costrini discloses a method of making a magnetic tunnel junction device (paragraph 0011), including forming a first mask layer (60)

(paragraph 0017; Figure 3) on the magnetic tunnel junction stack (100) (Figure 3); patterning the first mask layer (60) (paragraph 0017; Figure 3); forming a discrete magnetic tunnel junction stack by etching the first mask layer (60) (paragraph 0018; Figure 3); and forming a self-aligned via (66) by etching away the first mask layer (60) (paragraph 0023; Figure 6). Moreover, Costrini discloses that forming mask layer (60) enables the formation of a self-aligned vertical electrode to contact the underlying device (paragraph 0013). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of forming a first mask layer on the magnetic tunnel junction stack; patterning the first mask layer; forming a discrete magnetic tunnel junction stack by etching the first mask layer; and forming a self-aligned via by etching away the first mask layer. One who is skilled in the art would be motivated to form an etch mask as part of a process to form a self-aligned vertical electrode to contact the underlying device.

26. As to claim 2, Lee II claims that the depositing of the first electrically conductive material is continued until the first electrically conductive material completely fills the self-aligned via and the first electrically conductive material extends outward of the substantially planar surface by a predetermined distance (claim 2, page 4, lines 11-13).

27. As to claim 3, Lee II claims that the spacer layer is conformally deposited on the discrete magnetic tunnel junction stack (claim 3, page 4, lines 15-16).

28. As to claim 4, Lee II claims that spacer layer comprises a material selected from the group consisting of silicon oxide and silicon nitride (claim 4, page 4, lines 18-20).

29. As to claim 5, Lee II claims that the anisotropically etching the spacer layer comprises a reactive ion etch (claim 5, page 4, lines 22-23).

30. As to claim 6, Lee II claims that after the forming of the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other (claim 6, page 4, lines 25-27).

31. As to claim 7, Lee II claims a method of making a magnetic tunnel junction device from a previously fabricated discrete magnetic tunnel junction stack (claim 7, page 5, lines 1-2), comprising: forming an electrically non-conductive spacer layer on the previously fabricated discrete magnetic tunnel junction stack (claim 7, page 5, lines 4-5); forming a spacer by anisotropically etching the spacer layer (claim 7, page 5, line 7); forming a dielectric layer over the previously fabricated discrete magnetic tunnel junction stack and the spacer (claim 7, page 5, lines 9-10); planarizing the dielectric layer to form a substantially planar surface (claim 7, page 5, line 12); forming a self-aligned via by etching (claim 7, page 5, line 16); depositing a first electrically conductive material on the dielectric layer and in the self-aligned via (claim 7, page 5, lines 18-19); patterning the first electrically conductive material (claim 7, page 5, line 27); and forming a dual-damascene conductor by etching the first electrically conductive material (claim 7, page 5, line 27).

32. Lee II does not expressly claim forming a self-aligned via by etching away a first mask layer of the previously fabricated discrete magnetic tunnel junction stack. However, Costrini discloses a method of making a magnetic tunnel junction device (paragraph 0011), including forming a self-aligned via (66) by etching away the first

mask layer (60) (paragraph 0023; Figure 6) of the previously fabricated discrete magnetic tunnel junction stack. Moreover, Costrini discloses that forming mask layer (60) enables the formation of a self-aligned vertical electrode to contact the underlying device (paragraph 0013). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a self-aligned via by etching away a first mask layer of the previously fabricated discrete magnetic tunnel junction stack. One who is skilled in the art would be motivated to form an etch mask as part of a process to form a self-aligned vertical electrode to contact the underlying device.

33. As to claim 8, Lee II claims that the depositing of the first electrically conductive material is continued until the first electrically conductive material completely fills the self-aligned via and the first electrically conductive material extends outward of the substantially planar surface by a predetermined distance (claim 8, page 6, lines 1-3).

34. As to claim 9, Lee II claims that the spacer layer is conformally deposited on the previously fabricated discrete magnetic tunnel junction stack (claim 9, page 6, lines 5-6).

35. As to claim 10, Lee II claims that the spacer layer comprises a material selected from the group consisting of silicon oxide and silicon nitride (claim 10, page 6, lines 8-10).

36. As to claim 11, Lee II claims that the anisotropically etching the spacer layer comprises a reactive ion etch (claim 11, page 6, lines 12-13).

37. As to claim 12, Lee II claims that after the forming of the self-aligned via, the previously fabricated discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other (claim 12, page 6, lines 15-17).

Claim Rejections - 35 USC § 102 or 103

38. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. Claims 1-5 and 7-11 are rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Costrini.

41. As to claim 1, Costrini discloses a method of making a magnetic tunnel junction device, comprising: forming a magnetic tunnel junction stack (100) (paragraph 0011; Figure 2B); forming a first mask layer (60) (paragraph 0017; Figure 3) on the magnetic tunnel junction stack (100) (Figure 3); patterning the first mask layer (60) (paragraph 0017; Figure 3); forming a discrete magnetic tunnel junction stack by etching the first mask layer (60) (paragraph 0018; Figure 3); forming an electrically non-conductive spacer layer (72) on the discrete magnetic tunnel junction stack (paragraph 0020; Figure 4); forming a spacer (82) by anisotropically etching the spacer layer (72)

(paragraph 0020; Figure 5); forming a dielectric layer (86) over the discrete magnetic tunnel junction stack and the spacer (82) (paragraph 0023; Figure 6); planarizing the dielectric layer (86) to form a substantially planar surface (paragraph 0023; Figure 6); forming a self-aligned via (66) by etching away the first mask layer (60) (paragraph 0023; Figure 6); and depositing a first electrically conductive material (92/95) on the dielectric layer (86) and in the self-aligned via (66) (paragraph 0023; Figure 7).

42. Although Costrini does not expressly disclose patterning the first electrically conductive material and forming a dual-damascene conductor by etching the first electrically conductive material, these steps are an inherently present in forming the device. *See* Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002), pages 671-72, Figure 15-1. In the alternative, Applicant's claimed steps of patterning the first electrically conductive material and forming a dual-damascene conductor by etching the first electrically conductive material, would have obvious to one of ordinary skill in the art at the time the invention was made, because Wolf teaches these steps are commonly used in forming the final device structure.

43. As to claim 2, Costrini discloses that the depositing of the first electrically conductive material (92/95) is continued until the first electrically conductive material completely fills the self-aligned via (66) and the first electrically conductive material (92/95) extends outward of the substantially planar surface by a predetermined distance (paragraphs 0023, 0025; Figure 8).

44. As to claim 3, Costrini discloses that the spacer layer (72) is conformally deposited on the discrete magnetic tunnel junction stack (paragraph 0020; Figure 4).

45. As to claim 4, Costrini discloses that the spacer layer (72) comprises a material selected from the group consisting of silicon oxide and silicon nitride (paragraph 0020).

46. As to claim 5, Costrini discloses that the anisotropically etching the spacer layer (72) comprises a reactive ion etch (paragraphs 0020; 0004).

47. As to claim 7, a method of making a magnetic tunnel junction device from a previously fabricated discrete magnetic tunnel junction stack, comprising: forming an electrically non-conductive spacer layer (72) on the previously fabricated discrete magnetic tunnel junction stack (paragraph 0020; Figure 4); forming a spacer (82) by anisotropically etching the spacer layer (72) (paragraph 0020; Figure 5); forming a dielectric layer (86) over the previously fabricated discrete magnetic tunnel junction stack and the spacer (82) (paragraph 0023; Figure 6); planarizing the dielectric layer (86) to form a substantially planar surface (paragraph 0023; Figure 6); forming a self-aligned via (66) by etching away a first mask layer (60) (paragraph 0023; Figure 6) of the previously fabricated discrete magnetic tunnel junction stack; and depositing a first electrically conductive material (92/95) on the dielectric layer (86) and in the self-aligned via (66) (paragraph 0023; Figure 7).

48. Although Costrini does not expressly disclose patterning the first electrically conductive material and forming a dual-damascene conductor by etching the first electrically conductive material, these steps are an inherently present in forming the device. *See* Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002), pages 671-72, Figure 15-1. In the alternative, Applicant's claimed steps of patterning the first electrically conductive material and forming a dual-damascene conductor by

etching the first electrically conductive material, would have obvious to one of ordinary skill in the art at the time the invention was made, because Wolf teaches these steps are commonly used in forming the final device structure.

49. As to claim 8, Costrini discloses that the depositing of the first electrically conductive material (92/95) is continued until the first electrically conductive material completely fills the self-aligned via (66) and the first electrically conductive material (92/95) extends outward of the substantially planar surface by a predetermined distance (paragraphs 0023, 0025; Figure 8).

50. As to claim 9, Costrini discloses that the spacer layer (72) is conformally deposited on the discrete magnetic tunnel junction stack (paragraph 0020; Figure 4).

51. As to claim 10, Costrini discloses that the spacer layer (72) comprises a material selected from the group consisting of silicon oxide and silicon nitride (paragraph 0020).

52. As to claim 11, Costrini discloses that the anisotropically etching the spacer layer (72) comprises a reactive ion etch (paragraphs 0020; 0004).

53. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Costrini, in view of Chen (U.S. Patent No. 6,627,913).

54. As to claims 6 and 12, Costrini does not expressly disclose that after the forming of the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other. However, Chen discloses a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) with spacers (50) (column 5, lines 6-7; Figure 5). Chen teaches that the spacers (50) function to alleviate problems with mask misalignment (column 5, lines 49-50), such as overetching along the side of

the magnetic tunnel junction stack (column 2, lines 25-30; Figure 2). Moreover, Chen teaches that with the presence of spacer (50) results in greater design tolerances in mask alignment (column 6, lines 14-17, lines 22-24; Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other. One who is skilled in the art would be motivated to adopt a process with greater design tolerances.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

EBC
June 7, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER